IN THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A semiconductor device comprising:

a plurality of multiplexers to select one of a positive and a negative transmitter pins as a selected transmitter pin; ~~and~~

a first comparator to compare a voltage of the selected pin with a first reference voltage to determine whether there is leakage at the selected pin;

a first plurality of termination resistors coupled to the positive transmitter pin; and

a second plurality of termination resistors coupled to the negative transmitter pin such that each of the first and second pluralities of termination resistors are tested with the first reference voltage and the first comparator.

2. (Original) The semiconductor device of claim 1, further comprising core logic circuitry to receive an output of the first comparator.

3. Canceled.

4. (Original) The semiconductor device of claim 1, further comprising a positive receiver pin and a negative receiver pin coupled to the positive and negative transmitter pins, respectively, to provide an analog loop back path.

5. Withdrawn.

6. Withdrawn.

7. Withdrawn.

8. Withdrawn.

9. (Currently amended) A method to test an input/output of a semiconductor device, the method comprising:

selecting one of a positive transmitter pin and a negative transmitter pin as a selected transmitter pin; ~~and~~

comparing a voltage at the selected transmitter pin with a first reference voltage using a first comparator in the semiconductor device to determine whether there is leakage at the selected transmitter pin;

selecting one or more of a plurality of termination resistors as selected termination resistors; and

testing the selected termination resistors with the first reference voltage and the first comparator.

10. (Original) The method of claim 9, further comprising selecting the first reference voltage out of a plurality of voltage supplies.

11. Canceled.

12. (Original) The method of claim 9, further comprising:

coupling a positive receiver pin and a negative receiver pin in the semiconductor device to the positive and negative transmitter pins, respectively, to provide an analog loop back path within the semiconductor device; and

sending a test pattern from the positive and negative transmitter pins to the positive and negative receiver pins.

13. Withdrawn.

14. Withdrawn.

15. Withdrawn.

16. Withdrawn.

17. Withdrawn.

18. (Currently amended) A computer system comprising:

a plurality of dynamic random access memory devices (DRAM); and

a chipset coupled to the plurality of DRAMs, the chipset including a semiconductor device that comprises

a plurality of multiplexers to select one of a positive and a negative transmitter pins as a selected transmitter pin; ~~and~~

a first comparator to compare a voltage of the selected pin with a first reference voltage to determine whether there is leakage at the selected pin;

a first plurality of termination resistors coupled to the positive transmitter pin; and

a second plurality of termination resistors coupled to the negative transmitter pin such that each of the first and second pluralities of termination resistors are tested using the first reference voltage and the first comparator.

19. Canceled.

20. (Original) The computer system of claim 18, wherein the semiconductor device further comprises a positive receiver pin and a negative receiver pin coupled to the positive and negative transmitter pins, respectively, to provide an analog loop back path.

21. Withdrawn.

22. (Original) The computer system of claim 18, wherein the semiconductor device is a memory controller.

23. (Original) The computer system of claim 18, wherein the semiconductor device is an input/output controller.

24. (Original) The computer system of claim 18, further comprising a processor coupled to the chipset.